REMARKS

Claims 1, 2, 6, 8-14, 16-25, 27-51, 53 and 57-74 have been allowed by the Examiner.

Claim 52 was rejected by the Examiner under 35 USC §102(b) as being anticipated by Dawson et al. (6,111,260). In support of this rejection the Examiner states at the bottom of page 2 of the Action:

> "The Dawson et al. patent (Dawson) discloses a method for implanting dopant atoms into a semiconductor substrate (figs. 1, 2, and col. 4, line 8-col. 7, line 63). The method comprises the of directing a beam of dopant atoms to a surface of the substrate with sufficient energy so that the dopant atoms are distributed to a predetermined depth from the surface of the substrate, the **energy, dose and pulse duration imparted by the beam sufficient to raise the temperature of the substrate atoms to permit annealing of the dopant atoms** (col. 7, lines 31-63)." (emphasis added)

It is respectfully submitted that the Examiner's statement reproduced above is not what Dawson et al. teaches anywhere in the text of patent 6,111,260, and certainly not at col. 7, lines 31-63.

From a reading of Dawson et al., no mention of "pulse duration" was found - Dawson only talks of the range of temperatures contributed by the ion beam and the maximum range of temperatures needed overall.

At col. 7, lines 31-35, Dawson et al. says:

> "Referring to FIG. 2 in conjunction with FIG. 1, a flow chart illustrates a process for implanting ions and simultaneously annealing a substrate wafer 116 using an ion implant device 100 **including a thermal energy**

system for annealing a semiconductor substrate during ion implantation." (emphasis added)

At col. 7, lines 36-50, Dawson et al. describes the placement of the substrate in the chamber and the preparation of the chamber.

At col. 7, lines 51-63, Dawson et al. says:

"Simultaneous ion implantation and thermal annealing 214 is performed **by activating heating unit 146 to supply a predetermined thermal energy or a predetermined temperature in step 216 AND ALSO** activating ion bombardment by the ion implant device 100 in step 218. During the ion implantation and thermal annealing 214 step, the ion implant device 100 applies and controls the thermal energy applied to the substrate wafer 116 during ion implantation to raise the temperature of the substrate wafer 116 to a level that is sufficient to activate impurities within the substrate wafer 116 when an ion beam is implanting ions to the wafer, **but the temperature is insufficient to activate impurities when the ion beam is inactive**." (emphasis added)

From col. 7, lines 51-63 of Dawson et al. it is clear that what is disclosed is that BOTH ion bombardment AND thermal energy are combined to activate the impurities in the wafer. There is no mention or suggestion that the ion bombardment supplies both the ions AND sufficient temperature to the wafer to activate the impurities.

To further support this conclusion as to the teaching of Dawson et al. attention is directed to col. 6, lines 19-23, it is stated:

"The end chamber 140 includes a heating unit 146 for annealing a wafer during the ion implantation process. In some embodiments, the heating unit 146 is a lamp heating device. In other embodiments, the heating

unit 146 is a resistance heating device." (emphasis added)

Then from col. 7, line 63 through col. 8, line 6, Dawson et al. states:

"For example, an implanted wafer that is conventionally processed using rapid thermal annealing at a temperature of 1000° C. to 1050° C. is processed at a much lower thermal energy using simultaneous ion implantation because the ion beam inherently supplies a high temperature, generally approximately 200° C. but up to 500° C. for high voltage-high current beams. Accordingly, **thermal processing** that is performed simultaneously with ion implantation supplies a substantially reduced thermal energy to the substrate wafer 116. For an implanted wafer that is conventionally processed using rapid thermal annealing at a temperature of 1000° C. to 1050° C. a reduced-temperature annealing at temperatures from 400° C. to 800° C. may be supplied." (emphasis added)

While the preceding quotation indicates that Dawson et al. recognized that the implantation ion beam supplies some heat to the wafer, that heat amounts to no more than about one-fifth to one-half the temperature that is required and **thus thermal processing must be performed simultaneously to make up the difference required.**

What Dawson et al. is actually saying from col. 7, line 63 through col. 8, line 6, is that they have invented a method whereby much less heat needs to be supplied by a thermal source than that required with conventional rapid thermal annealing.

Claim 52, that was rejected based on Dawson et al. calls for:

"A method for implanting dopant atoms into a semiconductor substrate comprising the step of directing a beam of dopant atoms to a surface of

the semiconductor substrate with sufficient energy so that the dopant atoms are distributed to a predetermined depth from the surface of the substrate, **the energy, dose and pulse duration imparted by the beam of dopant atoms** being **sufficient to raise the temperature of the substrate atoms to permit annealing of the dopant atoms.**" (emphasis added)

That is not what Dawson et al. taught or suggested in their patent.

Thus it can be seen that claim 52 is clearly distinguishable from the teaching of Dawson, et al. Therefore claim 52 is now patentably distinguishable from the cited references and allowable.

All claims now being allowable, it is respectfully requested that the Examiner issue a Notice of Allowability for the above identified application.

Favorable action is respectfully requested.

Respectfully submitted,
Andrew M. Hawryluk et. al

by _____
Allston L. Jones
Reg. No. 27,906

Peters, Verny, Jones & Schmitt, L.L.P.
385 Sherman Ave., Suite 6
Palo Alto, CA 94306
Voice: 650/324-1677
FAX: 650/324-1678
e-mail: ajones888@earthlink.net
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